The readout controller for the calibration system of the Muon g-2 experiment

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***Abstract*—The Muon g-2 Experiment at Fermilab will measure the muon anomalous magnetic moment a=(g-2)/2 to an unprecedented precision of 0.14 parts per million (ppm). To this aim, a calibration system made by a laser source and light distribution will provide short light pulses directly into each crystal of the 24 calorimeters to measure energy and arrival time of the decay positrons. Each calorimeter is composed of a 6×9 matrix of PbF_2 crystals where each crystal is read by a Silicon Photomultiplier. Continuous monitoring and state-of-the-art calibration are required in order to control the detector response. The calibration light pulses are monitored, both at the laser output (Source Monitor) and at the end of the distribution system (Local Monitor), before delivery to the calorimeters. Namely, the light pulses are read by specific photodetectors, whose signals are digitized by electronics designed to match the experimental requirements. All readout electronics boards are hosted in a crate where the Controller manages the complete data collection, operates as an event-builder and transfers data to the online farm system through a gigabit ethernet connection. This data acquisition system is designed around a custom protocol and hardware to achieve high data transfer rate and event-building capability without software overhead. In this paper, after a general outline of this DAQ system, we describe in details the main features of Controller.**

***Index Terms*—Calibration, data acquisition, FPGA**

I. Introduction

THE E989 experiment[1],[2] at Fermilab plans to measure the muon anomalous magnetic moment to an uncertainty of 1.6×10^{-10} (0.14 ppm), derived from a 0.10 ppm statistical error and roughly equal 0.07 ppm systematic uncertainties on the knowledge of the precession frequency and the magnetic field.

The experiment efficiently uses the unique properties of the Fermilab beam complex to produce the necessary flux of muons, which will be injected and stored in the muon storage ring. To achieve a statistical uncertainty of 0.1 ppm, the total data set must contain more than 1.8×10^{11} detected positrons with energy greater than 1.8 GeV and arrival time greater than 30 μs after injection into the storage ring. The proton bunch hits a target in the antiproton area, producing a 3.1 GeV/c pion beam that is directed along a 900 m decay line. The resulting pure muon beam is injected into the storage ring.

The experiment benefits from upgraded detectors, electronics and data acquisition equipment to handle the much higher data volumes and slightly higher instantaneous rates. The positron detector system consists of 24 electromagnetic calorimeter stations placed on the inside radius of a magnetic storage ring. It must accurately measure the hit times and energies of the positrons which curl to the inside of the ring following muon decay. For maximum acceptance, the calorimeters are located partly within the storage ring's highly uniform 1.45 T magnetic field and extend radially inward to a region where the field falls to about 0.8 T.

A calorimeter station consists of 54 lead fluoride (PbF_2) crystals in an array that is 6 high and 9 wide, with each crystal read out on the rear face using a large-area Silicon Photomultiplier (SiPM) coupled directly to the crystal surface. In order to calibrate the calorimeter stations a laser system is used. To achieve a systematic uncertainty of 0.07 ppm, the response of each of the 1296 channels must be calibrated and monitored to limit the gain fluctuation at level of 10^{-4} in the time window 0-700μs into a muon fill [2], [3]. Over longer time scales, the gain should be stable at level of 10^{-3} to provide a reference value.

A calibration system, able to provide short laser pulses directly to each calorimeter crystal through a chain of optical fibers and other optical elements, has been realized[4]. The calibration system also includes a network of photodetectors with specialized electronics to manage signal processing and data readout.

In this paper we present the data acquisition system (DAQ) of the calibration system of the Muon g-2 experiment that is based on a custom electronics board specifically designed to control the data taking. It implements the event-building functionality, offers DAQ monitoring services and performs slow control functions to manage photo-sensor and electronics. In Sec. II the calibration system is shortly described; the data readout from front-end modules and the event reconstruction are discussed in Sec. III. The implementation of the readout controller board is shown in Sec. IV. An integration test of all DAQ modules and the performance thereof is discussed in Sec V.

II. The calibration system

To illuminate all 1296 calorimeter crystals of the detector stations 6 laser will be used. In fact, the laser pulse should have similar characteristics of the Cherenkov light signal produced by positron showers in the crystals. The laser light pulses provide a reliable reference for positron energy measurement which can be used to normalize the response of different calorimeter elements. The light pulses should be stable in intensity and timing to allow the correction of systematic effects in the SiPM response.

The final design of laser calibration system is shown in Fig.

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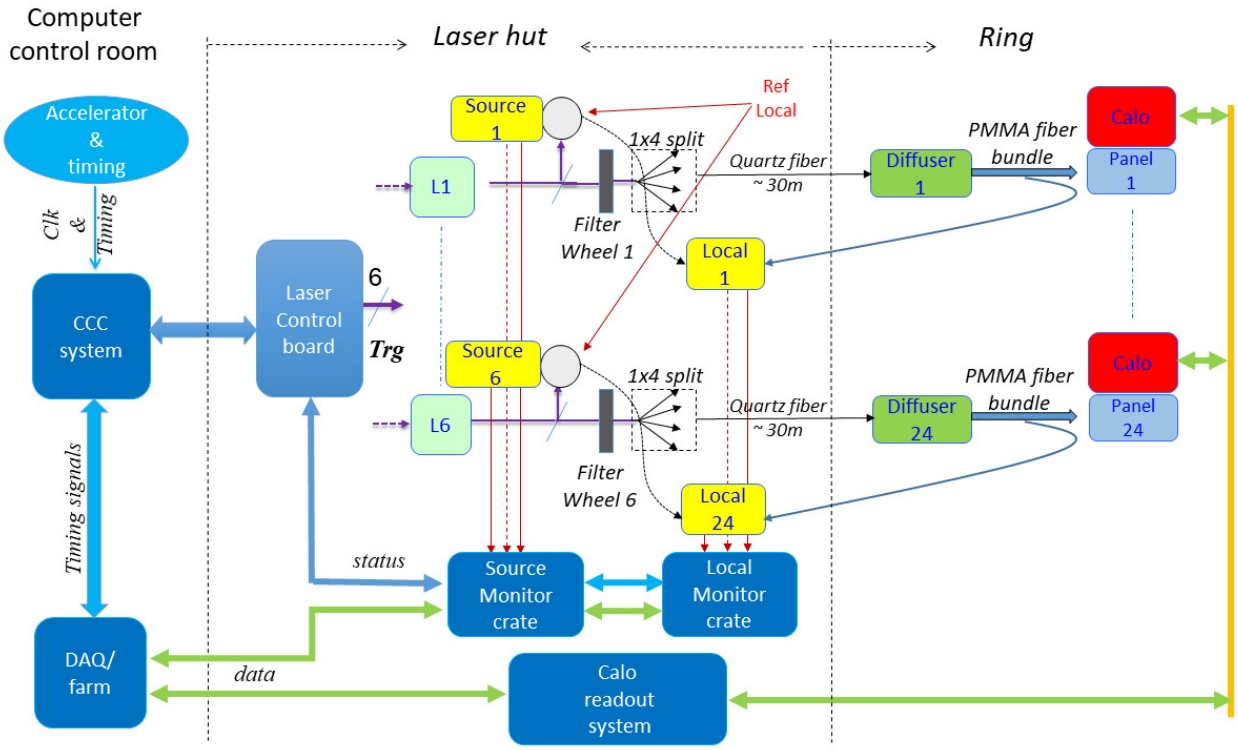

Fig. 1. The schematic diagram of Laser Calibration System. The light pulses are measured through the monitoring electronics both at the source and at the end of the distribution system. The data readout modules of the monitoring crates are located in the laser hut.

1 where the light source comes from six identical diode lasers (L1 and L6 boxes) manufactured by PicoQuant (LDH-P-C-405M), each of which has a maximum pulse energy of 1 nJ, a pulse width of about 700 ps at a wavelength of 405 $\pm$ 10 nm and a maximum repetition rate of 40 MHz. For each optical line, a beam splitter feeds 4 long quartz optical fibers. The output of each one is transmitted through a diffuser and then coupled into a bundle of optical fibers to illuminate uniformly all the calorimeter crystals. More details regarding design, implementation and test results of the light distribution system can be found in [4], [5], [6]. Time and amplitude fluctuations of the light source immediately at the beam exit are monitored by a Source Monitor (Source 1, Source 6 in figure) using thirty percent of the laser light. The light is measured by a redundant system of 2 large-area PIN diodes (PiDs) and a photomultiplier (PMT) via a wavelength shifter. The PMT is also coupled to a radioactive Americium source whose α particle passage into a scintillator provides an absolute reference light source. The transmitted light along the optical path to the crystals is measured to the delivery point with the Local Monitor (Local 1, Local 6 in figure). Its output pulse is compared with a reference pulse obtained by the Source Monitor. Each Local Monitor has a redundant system composed of two Photonics PMTs.

Specific electronics modules have been designed to manage the complete photo-detector data readout and to provide bias voltage and control signals. The modules are also able to register several temperature measurements and to run self-tests for calibration purposes of the electronics chain. All these modules are hosted in custom crates, as depicted in Fig. 1, and are fully controlled by master crate boards (see next sections).

The laser calibration program is defined inside the Laser Control Board[7]. It triggers the light pulses to the calorimeter stations and takes care of the interfaces between the monitoring system and the Trigger of the experiment. The laser pulse generation is operated with two different modes. The first is enabled, during physics runs, to correct for systematic effects due to drifts in the response of the light devices. The second is devoted to the test runs, without beam, in order to exercise the detector and DAQ when a specific pulse distribution is injected. A description of the Laser Control Board for light-based calibration system is in [8].

The data readout of the monitoring system must be able to accommodate several calibration modes and many types of light pulse generation in terms of pulse rate and data transfer.

III. The Data Acquisition for Calibration System

All calorimeter stations are readout via 12-bit waveform digitizers (WFDs) in μTCA crates [9]. Each SiPM channel is sampled at a rate of 800 MBPS and the data are transferred to a bank of GPU modules for on-line data processing[10].

The DAQ for the calibration system of the Muon g-2 experiment is based on a modular structure that is built around an event-driven data collection by using a custom bus protocol.

A. The Monitoring Board

Each crate of Source and Local Monitor, shown in Fig. 1, contains up to 12 boards, called Monitoring Board (MB), that

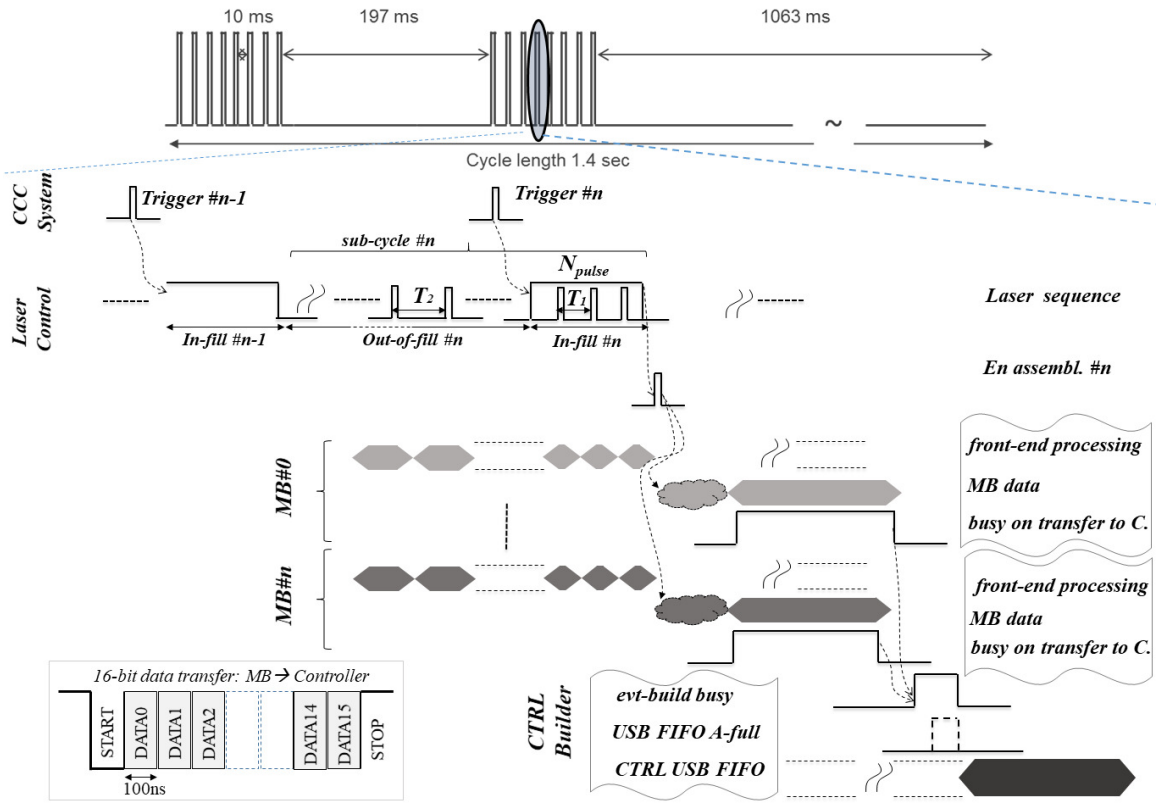

Fig. 2. Timing scheme of the data readout cycle. It includes data processing from front-end, data transfer to Controller (protocol based on a serial link depicted in the box at the bottom left) and complete event-building for a sub-cycle slot containing an "Out-of-fill phase" and an "In-fill phase".

manage the readout from up to 36 photodetector channels. Each MB has three independent sections to manage the same amount of photodetectors. In order to optimize the Signal to Noise Ratio (SNR), the input signal is integrated, amplified and filtered. A preamplifier circuit is the first stage in the processing chain. Then, a pulse shaper transforms the output from the preamplifier with a long tail (about 20 μs) to a semi-Gaussian shape around the peaking time. Reducing the pulse duration avoids the overlap and increases the signal rate. A baseline restorer is used to avoid the baseline shift causing an uncertainty in the peak determination.

Shaping and baseline restoration circuits feed an analog to digital converter (ADC) for digitization process. The ADC used for conversion is an Analog Device AD9244[11] with a 14 bit accuracy at 65 MSPS data rates. A peak detector is needed to track and hold the peak value long enough to allow the quantization process. In addition, the MB module provides the three filtered signals of photodetectors to the WFD boards to allow an independent digitization based on μTCA crate.

To improve the flexibility of electronics chain, the preamplifier circuit has been implemented on a daughter board near the sensor and connected with a data/control flat cable to the MB. This solution allows the use of a unique hardware platform to manage different photodetectors. The module, based on FPGAs, can be diversified (i.e. between Source and Local Monitor) by means of the loaded configuration files.

The MB processing and data readout activities do not require any external trigger. In fact, each channel is self-triggered and when the signal amplitude is greater than a threshold a data frame containing baseline measurement, peak value and time information is temporary stored in a buffer FIFO implemented inside the FPGA of the channel. The use of a threshold allows to cut-out very small signals.

A control section provides high voltage to the photodetectors by means of an 8 bit DAC with the possibility to read back the set values. Several temperature measurements are carried out with an accuracy of 0.1 °C, essential requirement in such a demanding monitoring system. Another important facility of the MB is the use of a test capacitance to inject charge on the line controlled by a 14 bit DAC that allows the self-calibration of each channel. This is mandatory for a monitoring system where the stability needs to be controlled at a sub-permil level.

All the frames of laser pulses, collected by MB during the same sub-cycle, are labeled by the event number (Trigger), packaged together with some auxiliary information and transferred to the crate controller. The operations regarding data transfer and communication to the Controller are executed in the fourth FPGA of the board placed near the backplane.

B. The readout cycle

The main cycle of the accelerator machine is represented by 16 repetitions of muon fill and decay windows (700 μs long, represented by the square signal in Fig. 2, or "in-fill phase") typically separated by 10 ms (or "Out-of-fill phase"). Actually there are two bunches of 8 filling-decay windows separated by about 200 ms and 1000 ms. The injection cycle repeats every

1.3 s. The data of the calibration system are organized for each sub-cycle containing an "Out-of-fill phase" and an "in-fill phase".

The readout chain is based on a trigger-driven algorithm where all MB slave boards and Controller share the same trigger signal coming from the CCC system. When a trigger arrives, each MB board performs the data assembling by collecting all the sub-frames from the three buffer FIFOs acquired during the sub-cycle (as shown in Fig. 2). A header with trigger number, control words and slow control information (temperature and bias measurements) is also attached. Such a reconstructed frame is pushed in a FIFO implemented in the fourth FPGA and then transferred to the Controller which in turn performs the event building at crate level. It processes all the sub-frames from MB slaves pertaining to the same trigger number, checks the data integrity, adds control and monitoring words and stores the frame in a FIFO accessible by an embedded processor for the final readout.

The Controller manages data collection from a maximum number of 12 slave boards. Each board is connected to a Controller by means of two unidirectional serial links (to send and receive). There are also some control signals that are broadcasted by the Controller to slave boards to implement the communication protocol (i.e. trigger signal, synchronization/reset signals, busy). Each slave, in case of an error condition occurred during the data taking, can assert a stop signal on a wired-OR line and the Controller starts a readout cycle to register the status of the boards.

The communication protocol between slave boards and Controller is inspired to RS-232 standard; the time slots are 100 ns long, each word has 16 bits with other two bits for start and stop of the word.

The input section of the Controller has 12 identical slices to manage the readout from slaves; in particular it reconstructs each slave's frame, checks its integrity and writes it into a buffer FIFO. The use of a buffer memory improves the decoupling between the input and output sections.

When all the data packets from the slave boards labeled with the same trigger number are written in the receiver FIFOs the event building block starts the parsing of sub-frames and pushes them into the building FIFO until the last board is reached. An embedded processor hosted on the board takes care of the final readout by means of high speed connections based on USB and sends data to the online farm for further proccessing.

In case of a multiple crates, several Controller boards can be chained together as shown in Fig. 3. All the control signals can propagate from the master Controller of chain to the last one. The event building at crate level is fully realized in hardware, while the final event building at chain level must be implemented at farm level. The laser calibration system of the Muon g-2 experiment consists of 2 or 3 crates one for Source Monitor and 1 or 2 for the Local Monitor.

IV. CONTROLLER IMPLEMENTATION

The Controller is a Single-Board-Computer that integrates an Artix7 FPGA by Xilinx [12], [13], [14] and an ARM-based Qseven processor [15]. The board has been designed to realize a flexible and scalable platform for applications oriented to control and monitor complex systems of sensors and detectors. The layout is shown in Fig. 4.

The board is equipped with an Artix-7 in a 676-pin ball grid array package. The newest generation of 7 series devices are built on advanced 28 nm process technology to produce the lowest-cost and lowest power FPGAs. The device used in the board is an XC7A200T-FBG676C with 215 k logic elements, 13 Mb of block RAM and 740 DSP slices and 500 I/O pins usable by the user.

The logic blocks that manage the data flow and buffering from the 12 slave boards to the full reconstruction of fragments in the USB FIFO, including control and monitoring activities, have been implemented in the FPGA in VHDL code.

A 230-pin card-edge MXM connector[16] provides a high speed signal interface between the FPGA device and the Qseven module. This connector is commonly used for high speed PCI Express graphics cards in notebooks. Qseven modules have a standardized form factor of 70 mm $\times$ 70 mm and a defined pinout that remains the same regardless of the vendor. In fact, it is possible to unplug the module and replace it with another in order to test different products or in case of different application and/or an upgrade.

In the present implementation, the Controller board is equipped with NXP i.MX6 Quad ARM Cortex A9[17] running at 1 GHz, a 4 GB onboard DDR3L memory and a 4-GB eMMC[18] solid-state storage controller. The module offers one PCI Express lane that supports PCI Express Gen. 2.0 interfaces at 5 Gb/s and a Gigabit Ethernet port. The Qseven module provides the functional requirements for an embedded application. These functions include one SATA port, multiple USB ports (via USB2.0 host controllers), one UART interface, two RS-232 interfaces onboard and several GPIO pins.

Qseven modules support different operating systems: Android, Linux and Windows Embedded Compact. Debian 7 version has been installed on the Controller module. The kernel and the root filesystem (rootfs) can be loaded via network or locally from eMMC or SD card.

Several specialized tasks running on the Qseven module are the core of the software architecture for data readout and monitoring of detectors and DAQ modules. In the present version, the data reconstructed by the event building logic are transferred from the FPGA FIFO to a high speed EZ-USB FX2LP (CY7C68013A by Cypress)[19] device implementing USB2.0. The EZ-USB FX2LP operates at data rate up to 480 Mbps by using endpoint FIFOs and slave FIFOs which interface to the FPGA logic. The EZ-USB FX2LP chips offers an integrated, high-performance CPU based on 8051 microprocessor with 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs. The embedded CPU is not used directly in the data transfer but it configures the device interfaces and modes. The collector process, based on libusb[20] library, continuously reads the 512-byte endpoint FIFO using bulk transfer.

The control and monitoring tasks are distributed to the Controller through serial links. These tasks are used to initialize the hardware modules, to check the status of electronics blocks

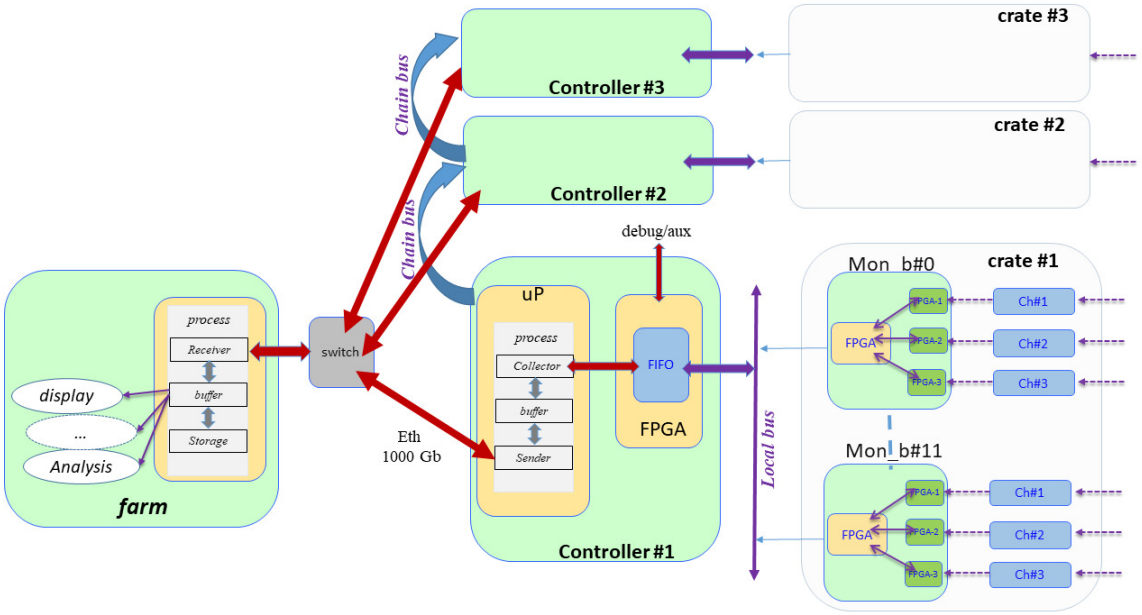

Fig. 3. DAQ chain for a multiple crate system. Each crate contains up to 12 slave boards that manage the readout from up to 36 photodetector channels. The Controller collects the slave data by using a custom bus and sends them to the online farm.

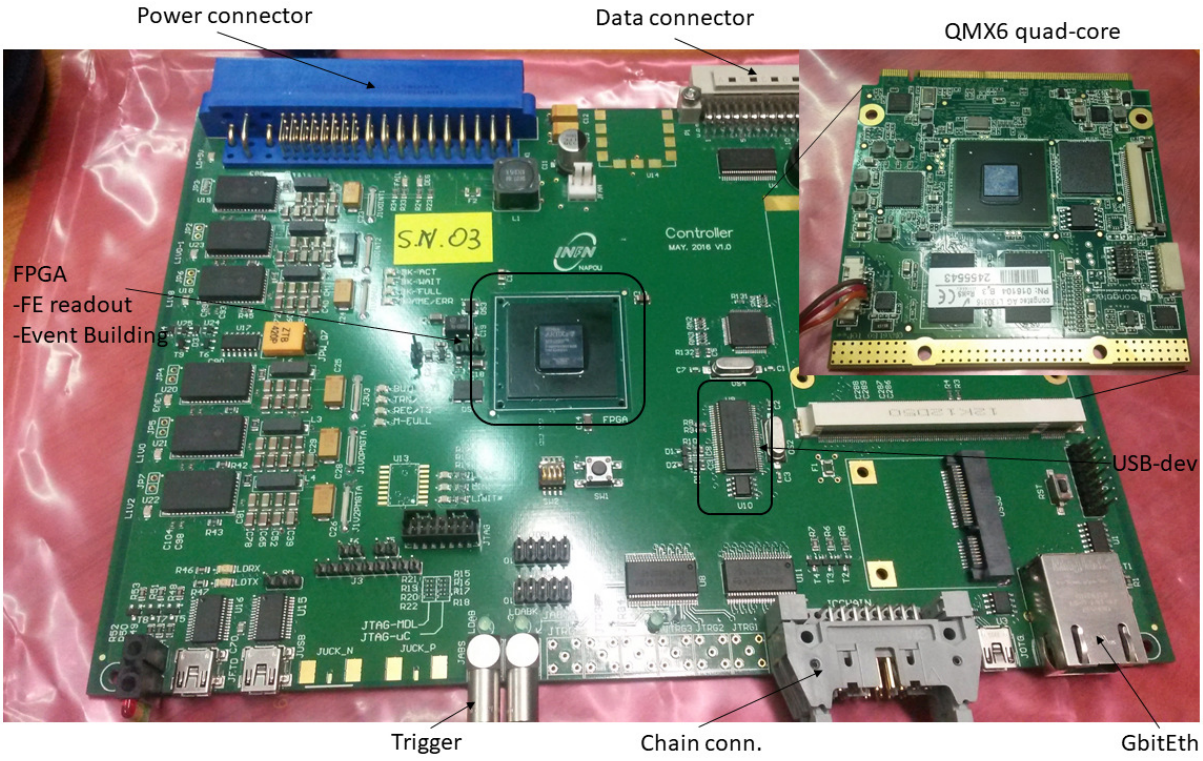

Fig. 4. Lay-out of Controller. It is based on a hybrid platform with FPGA and ARM-based processor.

and to manage run conditions.

V. Test results

A slice of the DAQ system was assembled at the Naples laboratory in order to integrate and test all the DAQ components under real conditions. One Source Monitor element containing 2 PiDs and one PMT was used to monitor light pulses from a PicoQuant LDH-P-C 405M pulsed diode laser. The signals from these three photodetectors were fanned-out to several copies to feed 3 MBs hosted in the DAQ crate with the Controller. The trigger logic was replaced by a pulse generator to simulate the beam cycle set at a rate of 100 Hz that exceeds the rate of the experiment. In the present setup, the software reads data from the Controller and sends them to the PC-server via gigabit-ethernet. Some monitoring activities can be enabled on the Controller to display the behavior of temperature and bias measurements or baseline and peak values of the light pulses. In addition, the processes for DAQ monitoring can be turned on to study the DAQ performance and tune it.

The amount of data for each cycle depends on the number of light pulses N_{pulse}. The data packet assembled each photodetector channel is made of 5 16-bit words/pulse that corresponds to 15 words/pulse per board. Moreover, the PMT counting rate is increased by a small amount due to the Americium signal with a rate of about 10 Hz. There is also a header of 25 words per board cycle containing slow control information.

In this set-up we measured the data transfer rate by changing N_{pulse} per cycle. Fig. 5 shows a linear behavior of the data transfer rates. The slave measurements are carried out by the receivers of the Controller. The data rate at the output of the Controller is measured by the collector firmware that is interfaced to the USB device. The maximum value of slave data transfer is $\sim$ 8 Mb/s (Fig. 5). By design the peak value is about 9 Mb/s.

Considering the maximum number of slave boards hosted in the crate, the data transfer from Controller is up to $\sim$ 12 Mbyte/s that is far below the USB 2.0 limit of 480 Mbps. Actually, the expected number of pulses for cycle should not exceed 100.

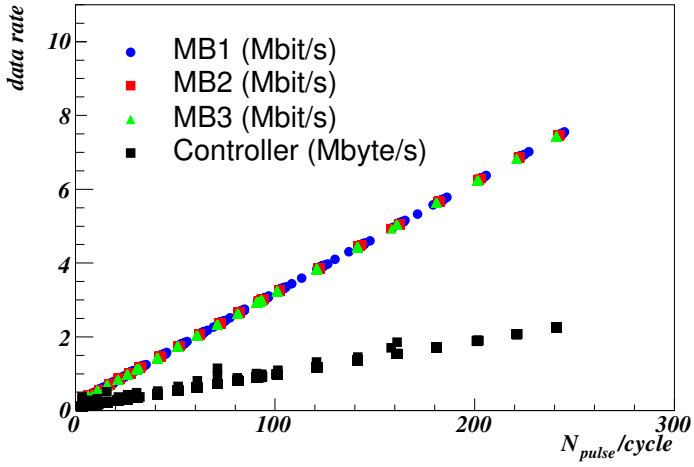

Fig. 5. *Data rate for MBs and Controller versus N_{pulse} per cycle. The measurements have been collected by Controller.*

The last part of this section is devoted to the DAQ monitoring able to track in real-time data frames shifting from slave boards to the Controller. As said, data transfer between slaves and Controller runs over serial links in synchronous mode with respect to the trigger signal. A busy signal is asserted for each slave transfer and its shape can be used to monitor it. Controller activities can be monitored with two signals as depicted in Fig. 2: a builder busy, asserted when the builder process is on, and a FIFO busy that is "1" when the Almost-Full FIFO flag is active. While slave busies and builder busy are fully ruled by the hardware, FIFO busy strongly depends on the software running on the CPU.

Therefore, in order to optimize the overall performance, avoid dead time, control the data collection and debug the anomalous data transfer it is essential to use a control instrument that monitors continuously (trigger based) several signals of the DAQ architecture. Duty cycle and toggle rate of all the busies are measured and attached to the data frame to be immediately correlated to the pulse pattern. Busy signals

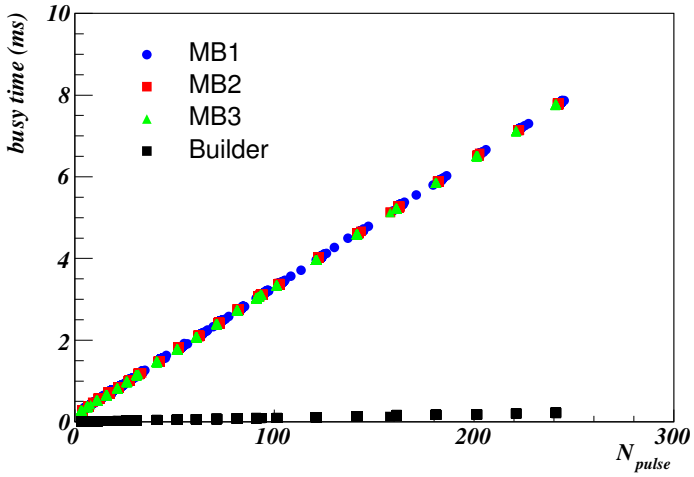

Fig. 6. *Duty cycle of MB and Builder busies for an event-driven data collection (see text for details).*

of the MBs and the Builder exhibit a linear behavior with respect to N_{pulse} as shown in Fig. 6. The time spent in the Builder process is smaller than MB data transfers. Fig. 7 shows the toggle rates for slave and USB FIFO busies. MB data transfer do not highlight interruptions and USB FIFO busy is always inactive meaning no dead time is introduced in the data acquisition.

The study of busy quantities demonstrates that data frames shift smoothly from MBs to Controller USB device through different levels of buffer FIFOs in a wide range of pulse rate without introducing any dead time.

VI. Conclusions

The Controller has been specifically designed to manage the readout from electronics boards for the Laser Calibration system of Muon g-2 experiment. The module is a Single-Board-Computer based on an Artix7 FPGA and an ARM

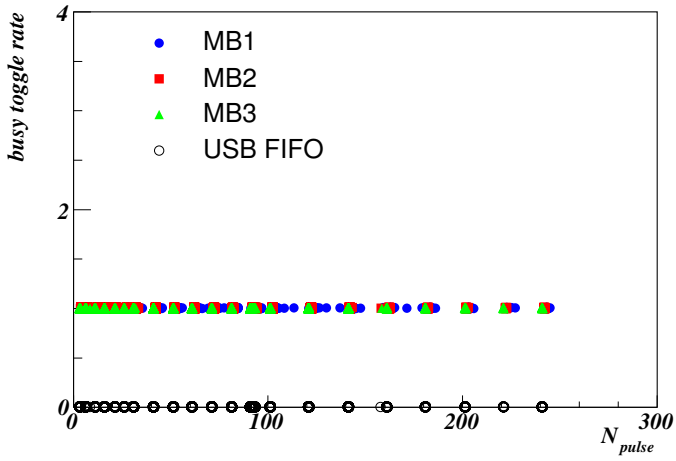

Fig. 7. *Toggle rates of MB busy signals asserted during data transfer to Controller and USB FIFO busy that becomes "1" with the rising edge of Almost-Full FIFO flag.*

Cortex A9 embedded processor which fulfills with hardware the first stage of event-building, a full data collection and an online processing.

The presence of an onboard CPU performs control and monitoring tasks of the hardware processes and allows a remote update of hardware platforms that is an essential requirement for applications operating in an limited-access area.

A complete readout system has been assembled and tested for several months at the Naples laboratory and then installed at Fermilab for the first engineering runs.

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