

# The Monitoring Electronic of the Laser Calibration system in the Muon g-2 experiment

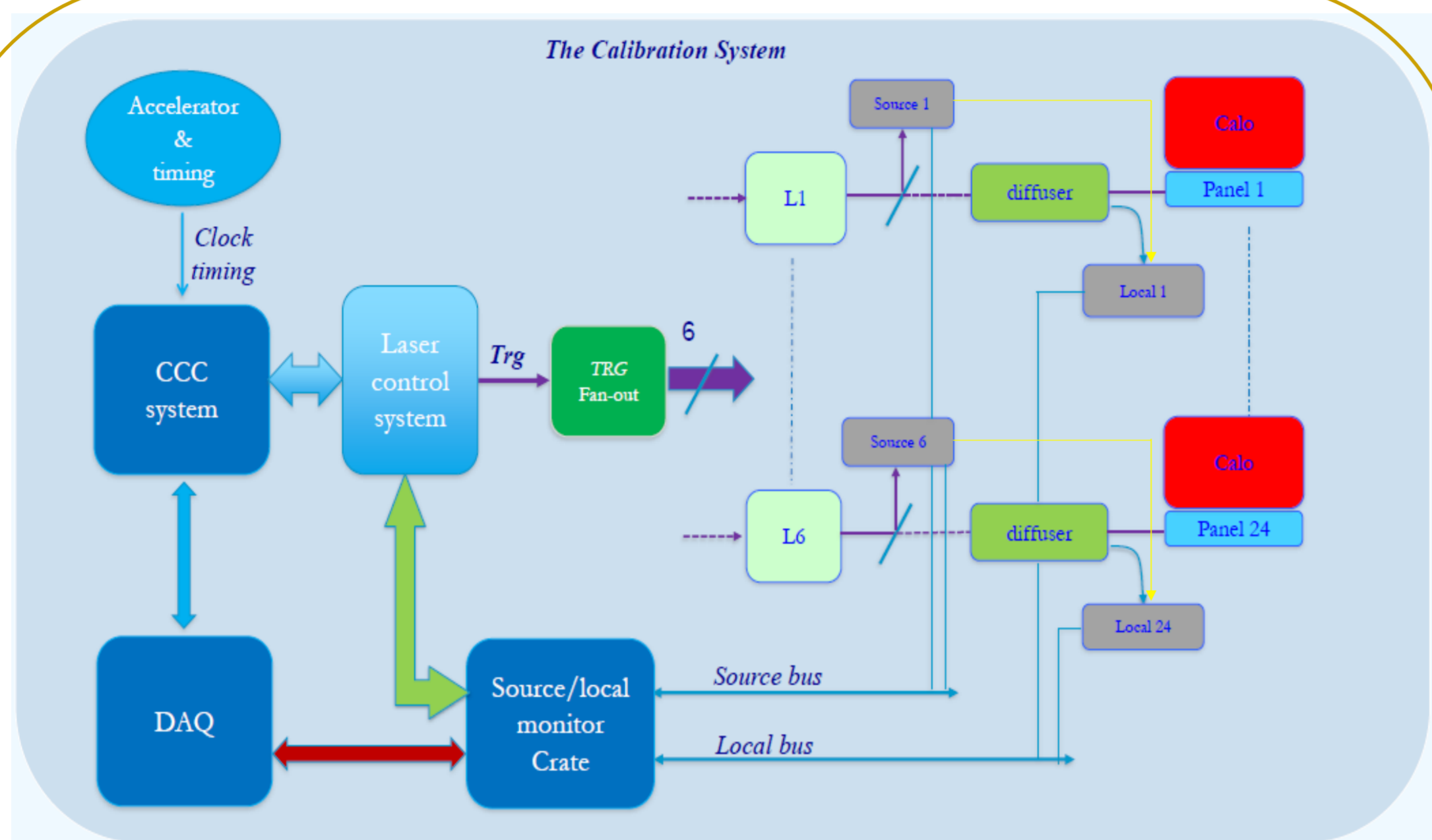
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on behalf of the Muon g-2 Collaboration

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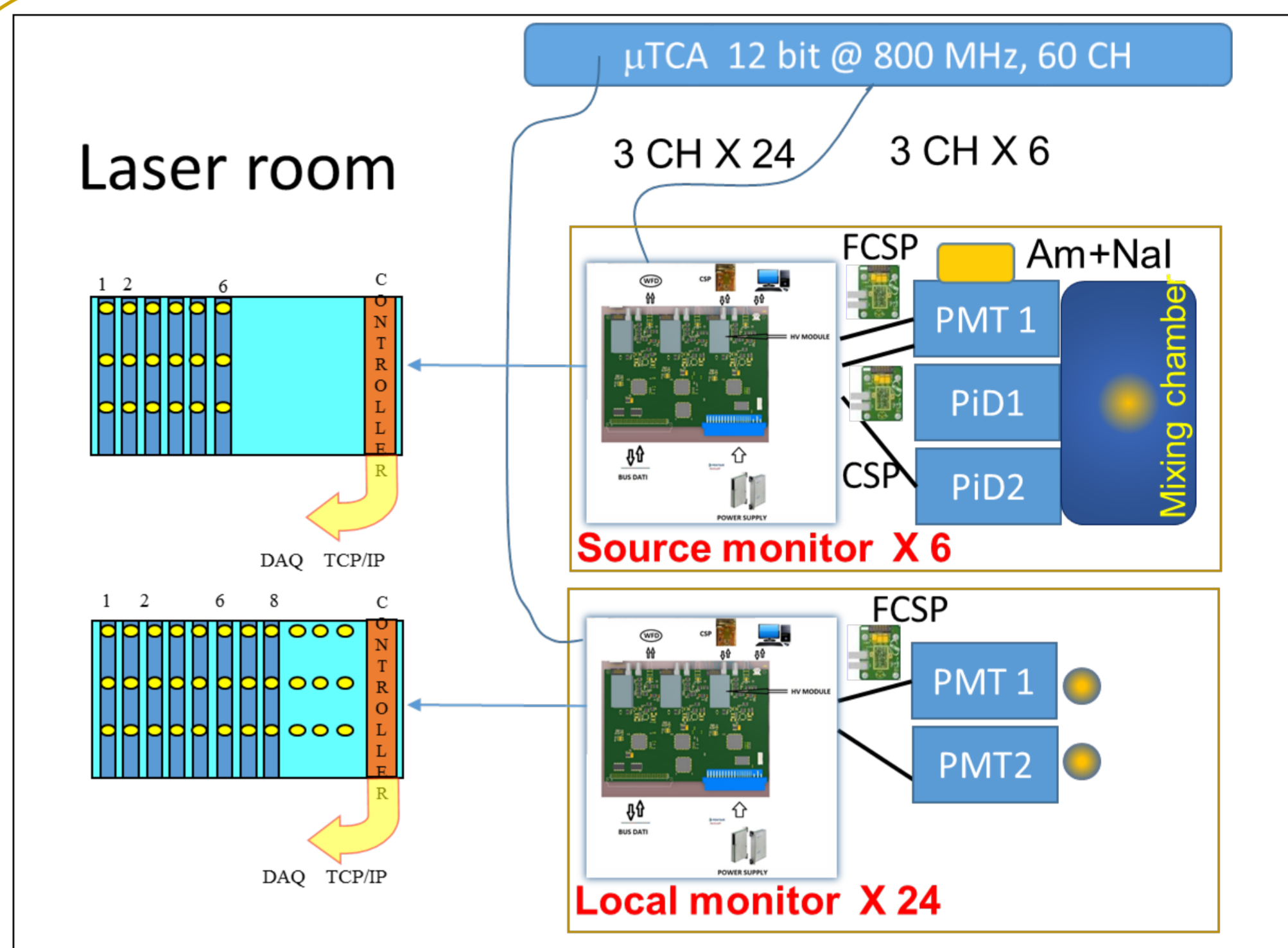
The new Muon g-2 experiment at Fermilab (E989) will measure the muon anomaly  $a_\mu = (g_\mu - 2)/2$  to an uncertainty of  $16 \times 10^{-11}$  (0.14 ppm), derived from a 0.1 ppm statistical error and roughly equal 0.07 ppm systematic uncertainties on the precession rate and magnetic field strength measurements. The experiment will run with a positive muon beam. The decay positrons will be detected by 24 electromagnetic calorimeters placed on the inner radius of a magnetic storage ring. They accurately measure arrival time and energy of the positron which curl to the inside of the ring following muon decay. Each calorimeter consist of 54 lead fluoride (PbF<sub>2</sub>) crystals in a 6 high by 9 wide array. To achieve a systematic uncertainty of 0.07 ppm, the gain fluctuation of each calorimeter channel must be contained to less than  $10^{-4}$ . To this aim a laser calibration system has been realized which is able to provide short laser pulses directly to each calorimeter crystal. The monitoring of these light signals is done by specific photo-detectors which translate the light pulse into electronic signal, which in turn is read by specialized Monitoring Electronics. The Monitoring electronics, organized in specific crates, performs full data acquisition of the calibration signals, starting from pre-amplification, then digitization of the signals and finally transfer of the information. Here we describe the whole system in its structure along with the main features of the component boards.

## Monitoring electronics and DAQ

### Laser Calibration System



The system consists of a laser control card (Laser control system), which is able to drive 6 lasers (L1, ... L6) which, via a distribution system (diffuser, 4 calorimeter / diffuser), provide light signals calibration to calorimeters (Calo). The light arriving at the calorimeters simulates the signal produced by the decay electrons of muons. The light produced by the laser is monitored at source (Source 1, .... Source 6) then downstream of the distribution (Local1, .... Local 24). These light signals are translated into electrical pulses by suitable detectors, then measured by special electronics (Electronic Monitoring).



The structure of SourceMonitor (SM) and LocalMonitor (LM) is depicted. In a SM the light enters into an integrating sphere, named "Mixing chamber" in the side picture, then it goes to 3 photo-detectors, namely 2 PIN diodes (PID, S3590-18) and one photomultiplier (PMT, H11900), all from Hamamatsu. The PMT is also coupled to a radioactive Americium-241 source embedded in a sealed NaI cristal. The  $\alpha$  particle crossing the scintillator provides an absolute reference light source.

In the LM the light of the 25 m-long PMMA fiber, which comes back to the laser room, starting from the diffuser exit, illuminates directly the two PMTs, as well a small fraction of light coming from the SM does. Therefore any change between these two signals is due to the distribution system. Specific electronics has been designed to read, process and digitize the signals coming from the SM and LM photo-detectors.

### Monitoring Board and Preamp

The SM and LM with their readout electronics and DAQ system are depicted in Fig. 3. Schematically, the signals from photo-detectors are preamplified (CSP, FCSP), then go to the Monitoring Board (MB) which performs filtering and digitization of the signal. The MBs are in custom crates containing up to 12 boards, each board has capability to manage 3 channels, moreover it is able to manage the photo-detector operation.

#### The preamplifier

The preamplifier circuit has been realized on a daughter board, completely separated from the main board, to allow flexible mechanical connection to the sensors. The pre-amplification is the first step of the processing chain, its design has required a careful coupling to the sensor and a noise reduction due to the dark current. The used S3590-18 PIN has an output capacitance ranging in tens of pF depending on the applied bias voltage. The signal from PIN devices are expected to vary from fraction of pC to several pC, with a rise time of about 10 ns and a fall time of hundreds of ns. The adopted configuration is based on a classical scheme, that is a cascade configuration with a feedback capacitor; the conversion gain (G) of the preamplifier was set to 800 mV/pC. A capacitor next to the channel input, chargeable by a process operated by the FPGA, allows self-calibration of the electronic channel. The preamplifier provides also a fast trigger which identify the arrival time of the signal, the same is made available, as an output signal, for other usage. For PMT signal, given the high gain of the detector itself, the gain is set to 200 mV/pC, while the preamplifier circuit is essentially the same as for PIN.

#### The pulse shaper and the baseline restorer

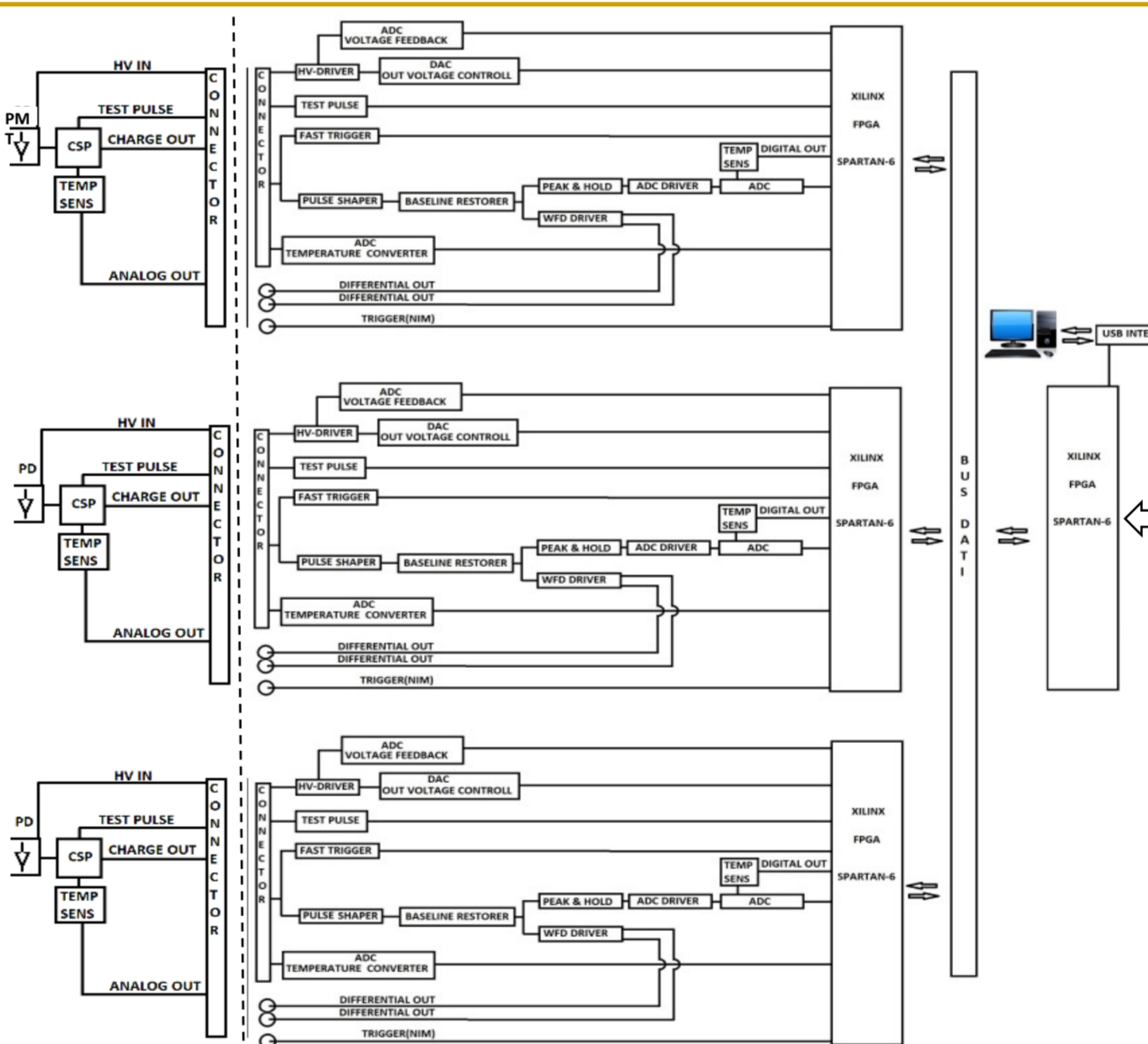
The pulse shaper circuit transforms the output from the preamplifier, which has a long tail (about 20  $\mu$ s), to a semi-Gaussian shape around the peaking time what reduces the pulse duration, avoids overlap and increases the sustainable signal rate. The analog components of this circuit have been chosen to obtain a pulse width of 600 ns. Next stage, the baseline restorer, is meant to avoid that baseline shift causes an uncertainty in the peak determination. The adopted scheme limits the pulse rate to a few tens of kHz. The output of the baseline restorer is doubled and one signal, made fully Gaussian with 600 ns width, is sent in a suited differential form to the WFD.

#### Peak detector and ADC conversion

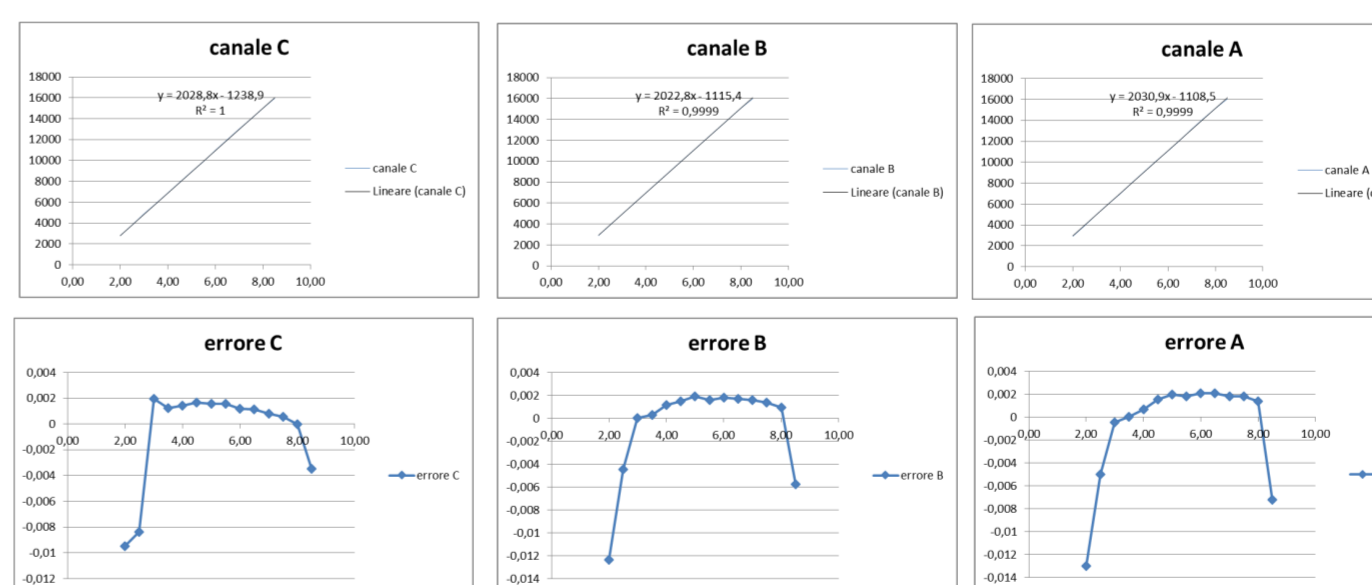
The other signal exiting the baseline restorer goes to a peak seeking circuit, which tracks and holds for long enough the peak value (P&H), then an analog to digital converter (ADC) converts the peak level. The chosen ADC is the AD9244 from Analog Device, it has a 14 bit accuracy at 65 MSPS data sampling. The differential input ranges from 0. to 2.0 V. The Effective Number of Bits (ENOB) is 11.7. The voltage drop rate of the P&H circuit is less than 30 mV/ms. Considering an acquisition time of about 400 ns the voltage drop is contained within 12 mV, that is well below 1 bit.

#### The FPGA control block

The signal processing of the photo-sensors is managed by the control-block represented by the FPGA. There is one FPGA per channel then 3 FPGAs on a board, namely #0, #1 and #2. The control block manages also the bias voltage for PINs and the reference voltage (HV) for PMT, the voltage is settable by an 8 bit DAC and the operational voltage can be readout back. For the PIN is used an EMCO module which is capable of relative voltage variation of few  $10^{-6}$  °C. Therefore the provided HV should be very stable as the room temperature is expected to be stable within 1-2 °C. For PMT the reference voltage (0-1 V) is generated by the board itself and is readout back over a shunt resistor. There are three temperature sensors for each channel: one located on the board (digitized value), another on the preamplifier board (analog signal) and the environmental temperature through an external sensor (digitized value). All sensors have an accuracy of 0.1 °C and are readout on request. The MB performs calibration of the 3 electronic channels by injecting a known charge at the preamplifier input, this process is operated through a 14 bit DAC. The MB activity do not require any external trigger; in fact readout is triggered when the signal amplitude is greater than a fixed threshold (Th1), then signal processing starts and data are stored in a local FIFO. On the PMT channel is implemented a 2.nd threshold (Th2) which allows distinction between laser and Americium signals. The FPGA of each channel builds the data frame for each pulse, which is made of header- cycle (machine) number, temperature and bias information-, then the sequence of signal information, that is pulse number, pulse time (measured with an accuracy of 10 ns) and the ADC value, finally a footer information. A further FPGA on a board, #3, reads the data frames from the three front-end FPGA and performs an event building at channel level. Then it sends data to the crate controller, via a fast link on backplane, that performs the complete event building and sends them to the data storage system. The MB module has also a slow interface (RS232) for debugging purposes.



Schematic of 3 readout Channels: preamplifiers (left) and SM Board (right)

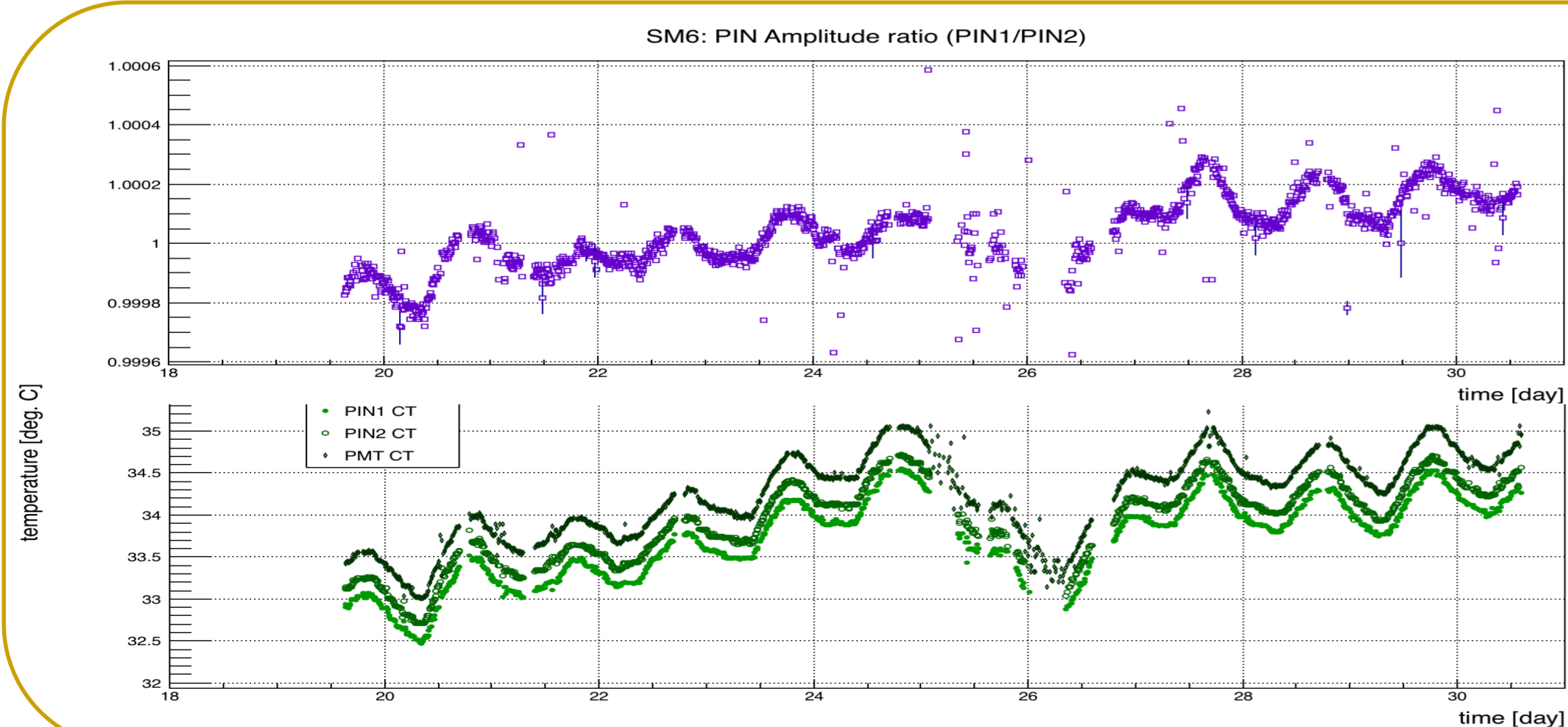


- MB sends signal to WFD, according to Common mode +/- 0.5 V at 1.9 V.
- Trigger: provides the LASER / Monitoring trigger to the WFD / DAQ
- Triggers the asynchronous transfers (Am) to  $\mu$ TCA / WFD
- Digitizes the monitoring signals with a 14-bit ADC and sends the values to the CONTROLLER which in turns provides the data to the DAQ via TCP / IP protocol.
- Digitization is started by the signal of the Laser Control (Start) suitably timed (programmable delay)
- Provides BiasV/HV to the detectors (PID/PMT) and monitor it
- Reads 3 Temp/channel (Tpreamp, Tboard, Tenv)
- Perform self-calibration of the electronic channel (known pulse at the preamplifier input)

Upper row: ADC count vs input voltage (V) for each of the 3 channels of the MB. Line is a linear fit, coefficients are reported

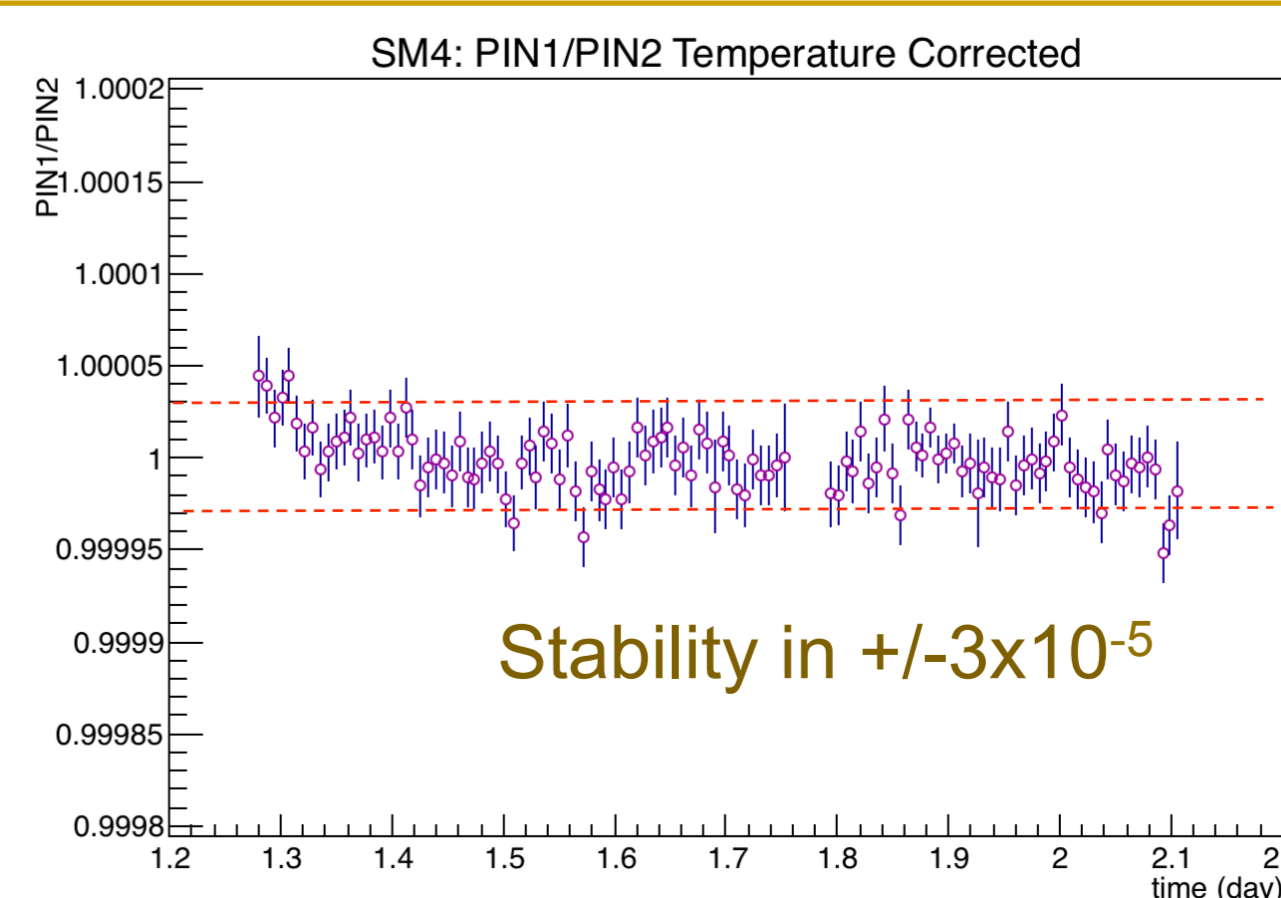
Lower row: Normalized residuals with respect to linear behaviour, or percentage error, vs input voltage (V) for each of the 3 channels.

## Performance



Upper Left : PIN ratio vs time (day) for 11 days of continuous data taking . This quantity should be independent of source and electronics variations, but it shows a correlation with Temperature. Its variation can be represented as following an environmental Temperature trend, plus a day night Temperature modulation.

Lower Left : Temperature behaviour as measured on the 3 preamplifier of the MB



PIN ratio after correction for Temperature dependence over 1 days of continuous data taking . It shows a stability at level of +/-3x10<sup>-5</sup>