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1. The Muon g-2 experiment

The new Muon g-2 experiment at Fermilab (E989) [1] measures the muon anomaly a_μ = (g-2)/2 to an uncertainty of 16 x 10^{-11} (0.14 ppm), derived from a 0.1 ppm statistical error and roughly equal 0.07 ppm systematic uncertainties on the precession rate and magnetic field strength measurements. The statistical precision requires 1.8x10^{11} accepted muon decay events. The proton bunch hits a target in the antiproton area, producing a 3.1 GeV/c pion beam that is directed along a 900 m decay line. The resulting polarized, almost pure muon beam is injected into the storage ring at a repetition rate of 12 Hz.
The experiment benefits from upgraded detectors, electronics and data acquisition equipment to handle the high data volumes and instantaneous rates. The experiment will run with a positive muon beam. The decay positrons will be detected by 24 electromagnetic calorimeters placed on the inner radius of a magnetic storage ring. They accurately measure arrival time and energy of the positron, which curl to the inside of the ring following muon decay. Each calorimeter consists of 54 lead fluoride (PbF2) crystals in a 6 high by 9 wide array, with each crystal read out on the rear face using a large-area SiPM coupled directly to the crystal surface. A 12 bit waveform digitizer samples the output signal of each photodetector at a rate of 800 MBPS then data are transferred to a bank of GPU processors for on-line data processing. The detectors and electronics are entirely new and a state-of-the-art calibration system will ensure performance stability throughout the long data taking periods.

2. The Muon g-2 Laser Calibration system

To achieve a systematic uncertainty of 0.07 ppm, the gain fluctuation of each calorimeter channel must be contained to less than 10^{-4} during the muon filling (0-700 μs) while over longer time scales, a gain stability of 10^{-3} would be sufficient.

To this aim a laser calibration system has been realized [2], [3], [4]. The calibration system is able to provide short laser pulses directly to each calorimeter crystal through a chain of optical fibers and other optical elements. These calibration pulses represent the normalization signals for the calorimeters, therefore they need to be monitored in order to guaranty their stability, and eventually react to any change. Possible variations might come from source instability or the distribution system itself, that's why the light is monitored both at the source (laser) and before delivery to the calorimeter (local). The monitoring of the light signals is done by specific photo-detectors which translate the light pulse into electronic signal, which in turn is read by specialized electronics.

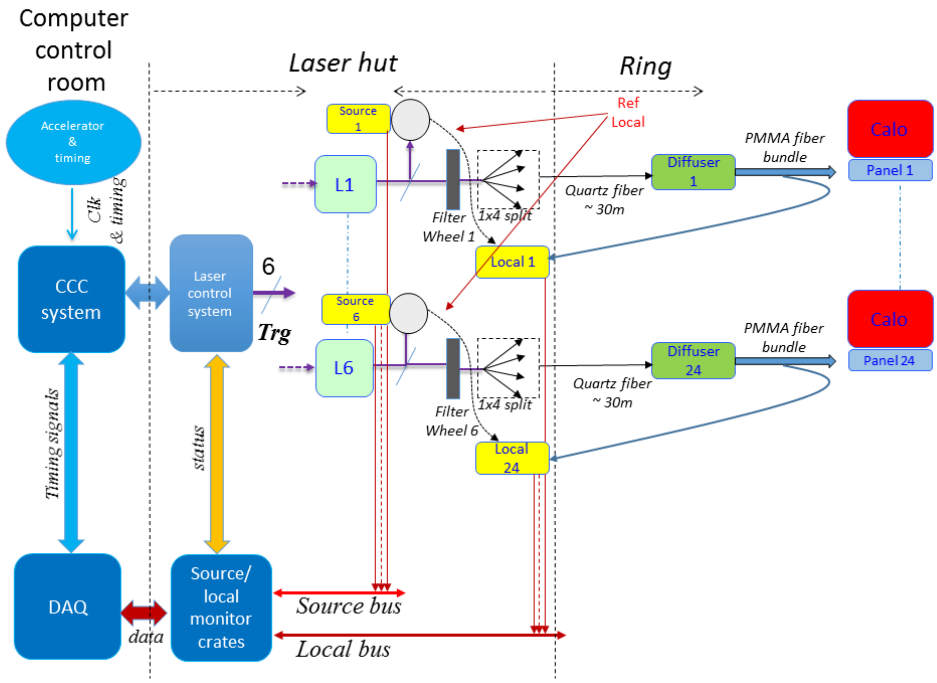

Figure 1: Schematic view of the Laser Calibration System. The system consists of a laser control card (Laser control, which is able to drive 6 lasers (L1, ... L6) which, via a distribution system (diffuser, 4 calorimeter / diffuser), provides light signals of calibration to calorimeters (Calo). The light arriving at the calorimeters simulates the signal produced by the decay positrons. The light produced by the laser is monitored at source (Source 1, ... Source 6) then downstream of the distribution (Local1, ... Local 24). These light signals are translated into electrical pulses by suitable detectors, then measured by dedicated electronics (monitoring electronic).

The implemented laser calibration system is shown in Fig. 1. The lasers are into a specific room, named laser hut, which is located just outside the ring. Within the laser hut there are six pulsed diode lasers Picoquant (LHD-C/D, PDL 200-B) whose light is divided at the exit by a beam splitter and part of it (20%) goes to the Source Monitor (SM), the yellow "Source n" box in the picture. The remaining (80%) is divided into four beams, each going through a 30 m-long quartz fiber to a diffuser which is coupled to a plastic fiber bundle where each fiber (2 m) serves a calorimeter cell. The light exiting few spare plastic fibers, suitably transported to the laser hut, is monitored by the Local Monitor (LM), the yellow "Local n" box. The LM also receives a small fraction of the light from the SM (smooth line named "reference local") which anticipates the previous one by about 220 ns.

A key element of the Laser Calibration system is the Laser Control board which acts as interface between the beam cycle and the calibration system, takes care of the laser pulse generation and distributes the time reference signals to the monitoring electronics.

The structure of SM and LM is depicted in Fig. 2. In a SM the light enters into an integrating sphere, named "Mixing chamber" in the side picture, then it goes to 3 photo-detectors, namely 2 PIN diodes (PID, S3590-18) and one photomultiplier (PMT, H11900), all from Hamamatsu. The PMT is also coupled to a radioactive Americium-241 source embedded in a sealed NaI crystal. The α particle crossing the scintillator provides an absolute reference light source.

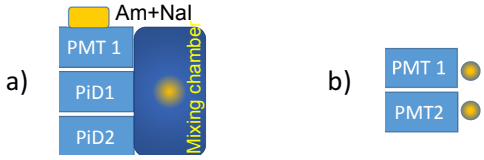

Figure 2: Schematic view of Source Monitor (a)) and Local Monotor (b)) detector structure. The photo-detectors receive light from an integrating sphere in case a) while directly from fiber in b).

In the LM the light of the 25 m-long PMMA fiber, which comes back to the laser hut starting from the diffuser exit, illuminates 2 PMTs, as well does a small fraction of light coming from the SM. Therefore, any change between these two signals is due to the distribution system.
Specific electronics has been designed to read, process and digitize the signals coming from the SM and LM photo-detectors.

3. Monitoring electronics and DAQ

The SM and LM with their readout electronics and DAQ system are depicted in Fig. 3. Schematically, the signals from photo-detectors are preamplified (CSP, FCSP), then go to the Monitoring Board (MB) which performs filtering and digitization of the signal. The MBs are in custom crates containing up to 12 boards, each board has capability to manage 3 channels, moreover it is able to manage the photo-detector operation.

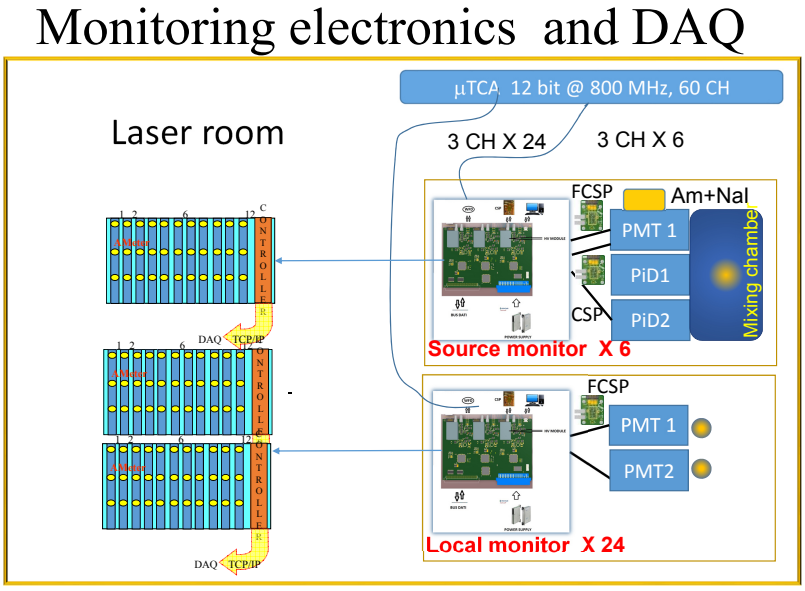

Figure 3: Schematic view of the Monitoring electronics and related DAQ system. The SM and LM are shown with their readout electronics: The signals to the microTCA (in the upper-right) hosting the WaveForm Digitizers are also shown. This represents a redundancy of the calibration signal monitoring. On the left are the crates where the Monitoring Boards are hosted; they perform the DAQ by a Controller board, which transfer data outside by a TCP/IP connection. The preamplifiers also are within the laser hut.

The MB is also able to register environmental/operational parameters, as temperatures and bias/HV voltage, to provide the operation voltage to the photo-detectors and to perform self-calibration of each electronic readout channel. All these modules are controlled by a crate Controller boards, which acts as data collector and sends data outside through a TCP/IP connection. Here we will describe the main features of the different board which make the Electronic Monitoring system.

3.1 The Laser Control Board

The LCB can be operated in different modes:
a) pulse train generation. In this mode trigger pulses to the lasers are provided at fixed and programmable frequency, both during the filling time window ("in-fill" pulses) and in absence of muons in the ring ("out-of-fill" pulses). In order to sample homogeneously all the time gaps, the pulse train is regularly shifted by a fraction of the pulse period;
b) physics event simulation, or "flight simulator" mode. The lasers are triggered according to an exponentially decreasing time distribution, $e^{-t/\tau}$, as in the experiment, reflecting the muon decay time distribution;
c) synchronization mode. A reference signal is sent to calorimeters by the laser, it serves as reset, synchronization and initialization of the detectors and their electronics.

The parameters to configure the operation mode are in an array of registers, accessible and settable by a software interface. Their nomenclature and meaning are synthetically shown in Fig. 4, where the accelerator machine cycle, which drives every timing, is also reported.
The LCB has been implemented by using a hybrid platform containing an FPGA board and an ARM-based processor; a schematic block diagram is shown in Fig. 5. The interface with the Clock and Control Center (CCC, that is the machine) is implemented in the Clock block where an external Trigger defines the beginning of the laser sequence. The Laser logic block distributes the signals to the laser drivers, fan-out multiplicity and time characteristics of pulses can be defined.

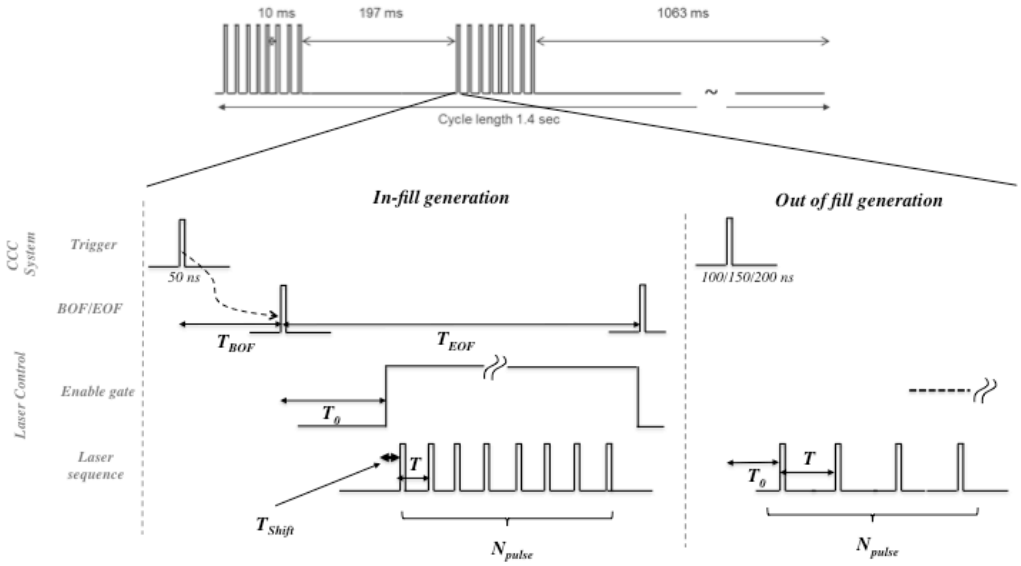

Figure 4: The main cycle of the accelerator machine and the generation of the pulse trains. The main cycle is represented by 16 repetitions of muon fill and decay windows (700 μs long, represented by the square signal in figure, or "in-fill phase") typically separated by 10 ms (or "Out-of-fill phase"). Actually, there are two bunches of 8 filling-decay windows separated by about 200 ms and 1000 ms. In the lower part is shown the laser pulse sequence, which is structured according to many self-explaining parameters [5].

The operation modes are managed in the Control Mode block. The control and monitoring operation of the LCB are managed by an ARM processor, whose components (RAM block, Ethernet and I/O peripherals) are depicted in Fig. 5. The communication between ARM and FPGA elements, used for configuration and monitoring, is based on Serial Peripheral Interface (SPI).

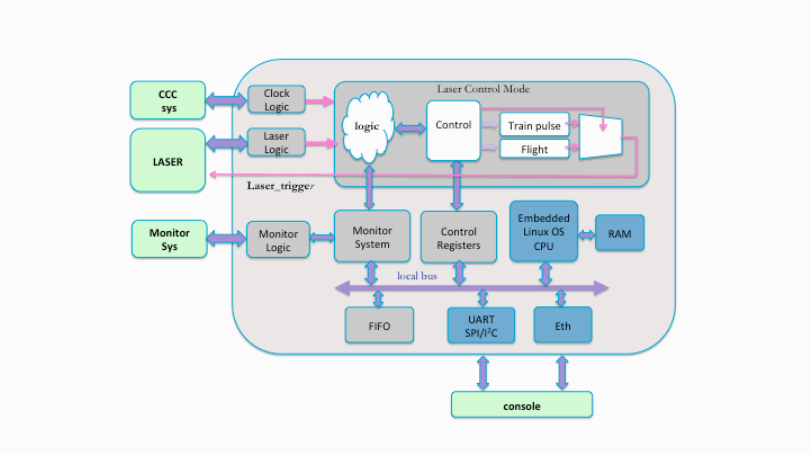

Figure 5: Block diagram of the LCB.

The generation of pulses for both "in-fill" and "out-of-fill" time windows is based on an enable gate. The programmable pulse rate ranges from hundreds of Hz to MHz. This mode is completely managed in hardware and needs only a setting of parameters.
In simulation mode, the LCB is able to repeatedly provide a time sequence and a mean number of pulses according to positron arrival time distribution, that is an exponential function like $A*e^{-t/\tau}$ with a characteristic time of 64.4 μs and a normalization factor A. The LCB contains two different implementations of the simulation mode.

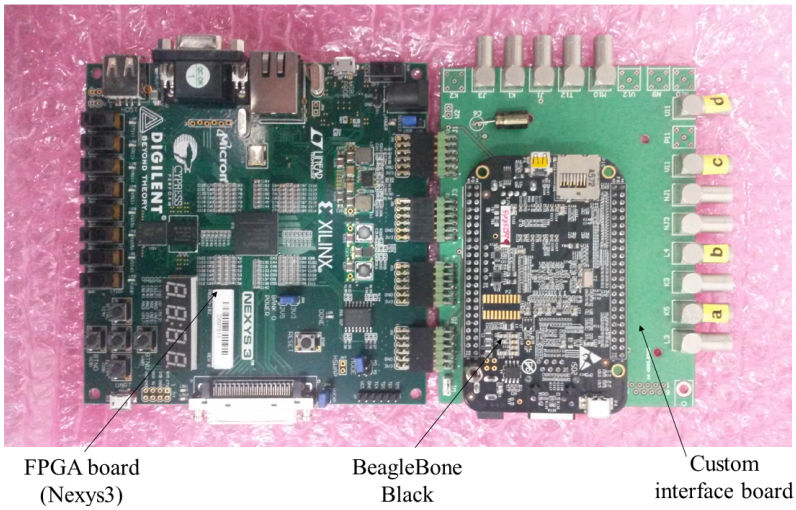

Figure 6: The LCB implemented by a Spartan6 FPGA board, a BeagleBone Black CPU and a custom board which plays as interface for signal exchange and component communication.

The first (HW) is fully realized in hardware (FPGA) while the second (SW&HW) consists of a CPU which generate random numbers and a hardware machine, implemented on FPGA, which generates the time sequences. Fig. 6 shows the implementation based on a Xilinx Nexys board and a BeagleBone ARM

processor. Fig. 7 shows a good agreement between the distributions of pulses obtained using the two implementations. This version has been used to do several tests on the SiPMs [6] and was recently used in different test beams in particular at LNF [7] and at SLAC test beam (2014 and 2016). The possibility to modify the number of pulses in a very large range allows important measurements on detector and DAQ performance.

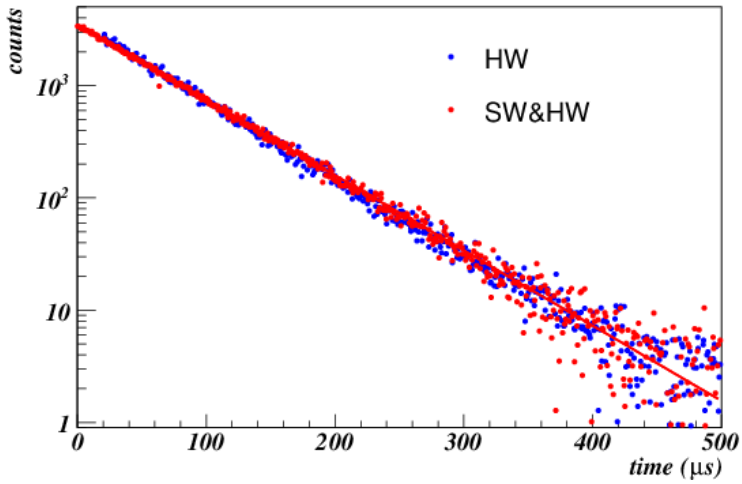

Figure 7: Time distribution of pulses generated according to an exponentially decreasing function "flight simulator" for the two implemented methods.

3.2 Monitoring Board

The Monitoring Board (MB) manages the signal processing and data readout of the photo-detectors, the block diagram of a single channel is shown in Fig. 8 along with the preamplifier. In order to optimize the Signal to Noise Ratio (SNR), the signal is integrated then amplified and filtered. The FPGA, by an implemented control logic, allows the setting up, operation and monitoring of processes managing the analog signals.

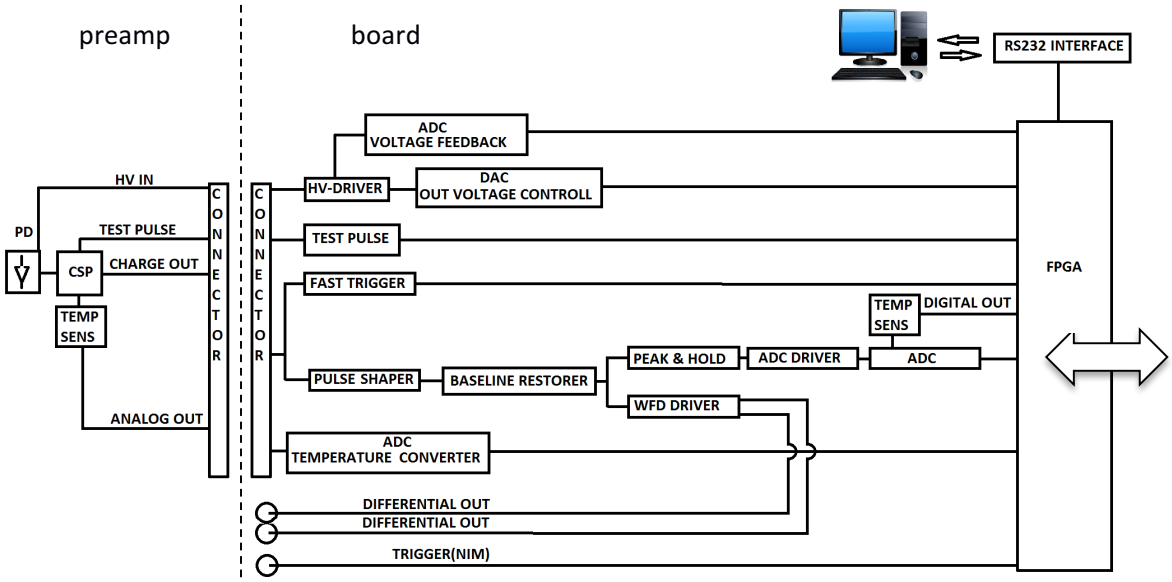

Figure 8: Preamplifier and SMB scheme for a single readout channel.

3.2.1 The preamplifier

The preamplifier circuit has been realized on a daughter board, completely separated from the main board, to allow flexible mechanical connection to the sensors, specifically the PIN which are soldered on it, while connection to PMT is through few cm of coaxial cable. The pre-amplification is the first step of the processing chain, its design has required a careful coupling to the sensor and a noise reduction due to the dark current. The used S3590-18 PIN has an output capacitance ranging in tens of pF depending on the applied bias voltage. The signal from PIN devices are expected to vary from fraction of pC to several pC, with a rise time of about 10 ns and a fall time of hundreds of ns. The adopted configuration is based on a classical scheme, that is a cascade configuration with a feedback capacitor; the conversion gain (G) of the preamplifier, defined as the ratio between the preamplifier output voltage and the input charge, was set to 800 mV/pC. A capacitor next to the channel input, chargeable by a process operated by the FPGA, allows self-calibration of the electronic channel. The preamplifier provides also a fast trigger which identify the arrival time of the signal, the same is made available, as an output signal, for other usage. For PMT signal, given the high gain of the detector itself, the gain is set to 200 mV/pC, while the preamplifier circuit is essentially the same as for PIN.

3.2.2 The pulse shaper and the baseline restorer

The pulse shaper circuit transforms the output from the preamplifier, which has a long tail (about 20 μs), to a semi-Gaussian shape around the peaking time what reduces the pulse duration, avoids overlap and increases the sustainable signal rate. The implemented scheme is based on a high-pass filter followed by low-pass filters; this circuit is referred as a CR-nRC shaper. The analog components of this circuit have been chosen to obtain a pulse width of 600 ns. Next stage is the baseline restorer. It is meant to avoid that baseline shift causes an uncertainty in the peak determination. This dc offset is generally caused by the amplifier gain with unipolar signal in case of high-counting rate (> tens of kHz). The adopted scheme limits the pulse rate to a few tens of kHz. The output of the baseline restorer is doubled and one signal, made fully Gaussian with 600 ns width, is sent in a suited differential form to the WFD.

3.2.3 Peak detector and ADC conversion

The other signal exiting the baseline restorer goes to a peak seeking circuit, which tracks and holds for long enough the peak value (P&H), then an analog to digital converter (ADC) converts the peak level. The chosen ADC is the AD9244 from Analog Device, it has a 14 bit accuracy at 65 MSPS data sampling. The differential input ranges from 0. to 2.0 V. The Effective Number of Bits (ENOB) is 11.7. The voltage drop rate of the P&H circuit is less than 30 μV/μs. Considering an acquisition time of about 400 ns the voltage drop is contained within 12 μV, that is well below 1 bit.

3.2.4 The FPGA control block

As shown in Fig. 8, the signal processing of the photo-sensors is managed by the control-block represented by the FPGA. There is one FPGA per channel then there are 3 FPGAs on a board, namely #0, #1 and #2. The control block manages also the bias voltage for PIN or the reference voltage (HV) for PMT, the voltage is settable by an 8 bit DAC and the operational voltage can be read back. For the PIN is used an EMCO module which is capable of relative voltage variation of few 10^{-6}/ °C. Therefore, the provided HV should be very stable as the room temperature is expected to be stable within 1-2 °C. For PMT the reference voltage (0-1 V) is generated by the board itself and is readout back over a shunt resistor. There are three temperature sensors for each channel: one located on the board (digitized value), another on the preamplifier board (analogical signal) and the environmental temperature through an external sensor (digitized value). All

sensors have an accuracy of 0.1 °C and are read on request. The MB board performs calibration of the 3 electronic channels by charge injection at the preamplifier input, this process is operated through a 14 bit DAC. The MB activity do not require any external trigger; readout is triggered when the signal amplitude is greater than a fixed threshold (Th1), then signal processing starts and data are stored in a local FIFO. On the PMT channel is implemented a second threshold (Th2) which allows distinction between laser and Americium signals.

The FPGA of each channel builds the data frame for each pulse, which is made of header- cycle (machine) number, temperature and bias information-, then the sequence of signal information, that is pulse number, pulse time (measured with an accuracy of 10 ns) and the ADC value, and a footer information. A further FPGA on the board, #3, reads the data frames from the three front-end FPGA and performs an event building at board level. Finally, it sends data to the crate controller, via a fast link on backplane, that performs the complete event building and sends them to the data storage system. The MB module has also a slow interface (RS232) for debugging purposes.

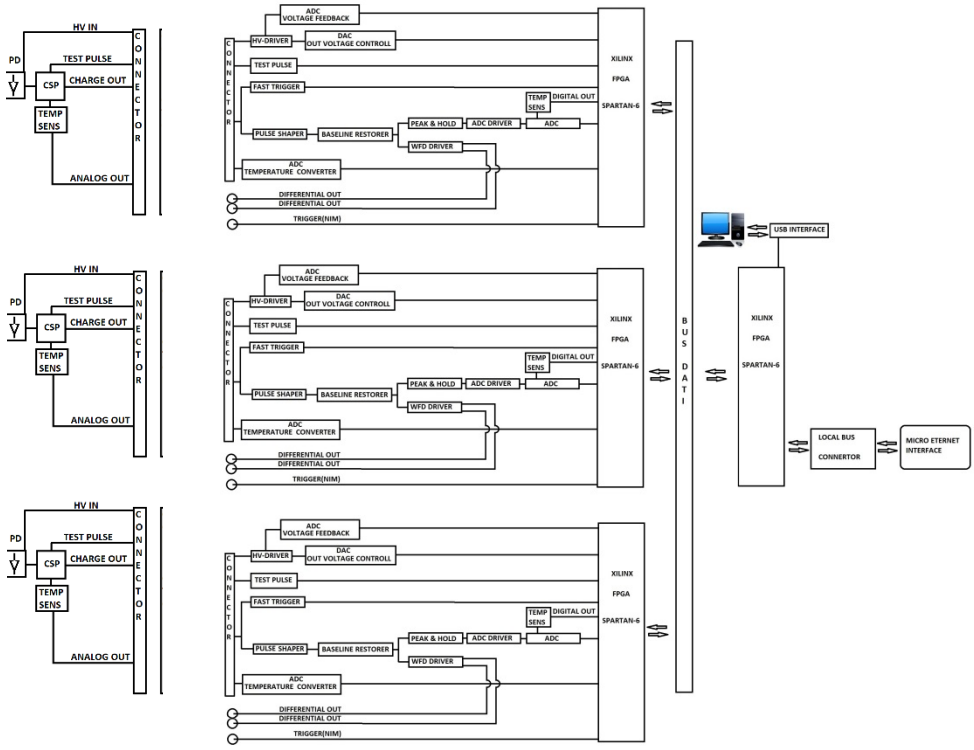

Figure 7: Schematic of preamplifiers (left) and SMB (right).

3.3 Controller board

The DAQ of the calibration signals is based on a modular structure and data readout is based on a trigger-driven logic where all MB (slave boards) and Controller (master) share the same trigger signal coming from experiment. When it arrives, each MB board performs the data assembling from the three channels, builds its data frame and then transfers it to the Controller which in turn performs the event building at crate level. It processes all data pertaining to the same trigger (event) number, checks the data integrity, adds control and monitoring words and stores the frame in a FIFO accessible by an embedded processor for the final readout. The Controller manages data collection from a maximum of 12 slave boards. Each MB is connected to the Controller by means of two unidirectional serial links (to send and receive). There are also

some control signals that are broadcasted by the Controller to the MB to implement the communication protocol (i.e. trigger signal, synchronization/reset signals, busy).
The communication protocol between slave boards and Controller is inspired to RS-232 standard; the time slots are 100 ns long, each word has 16 bits with other two bits for start and stop of the word. The input section of the Controller has 12 identical sub-sections to manage the readout from the slave boards.
An embedded processor, hosted on the Controller, takes care of sending data to the DAQ farm for further data processing. In case of multiple crates, the Controller boards can be chained together as shown in Fig. 3, where one Controller act as master and takes care of sending the control signals to the others. The event building at crate level is fully realized in hardware, while the final event building at chain level must be implemented at farm level. The Monitoring Electronics of the Muon g-2 experiment consists of 2(3) crates, 1 for Source Monitor and 1(2) for the Local Monitor.

4. Present status

At present a full crate of Source Monitor, shown in Fig. 8, is in operation on the experiment. Embedded into the crate is also the Laser Control Board. The first Local Monitor crate is going to be mounted at the experiment site and will be in operation by spring 2018, while the final decision for the construction of the second one will be made before summer.

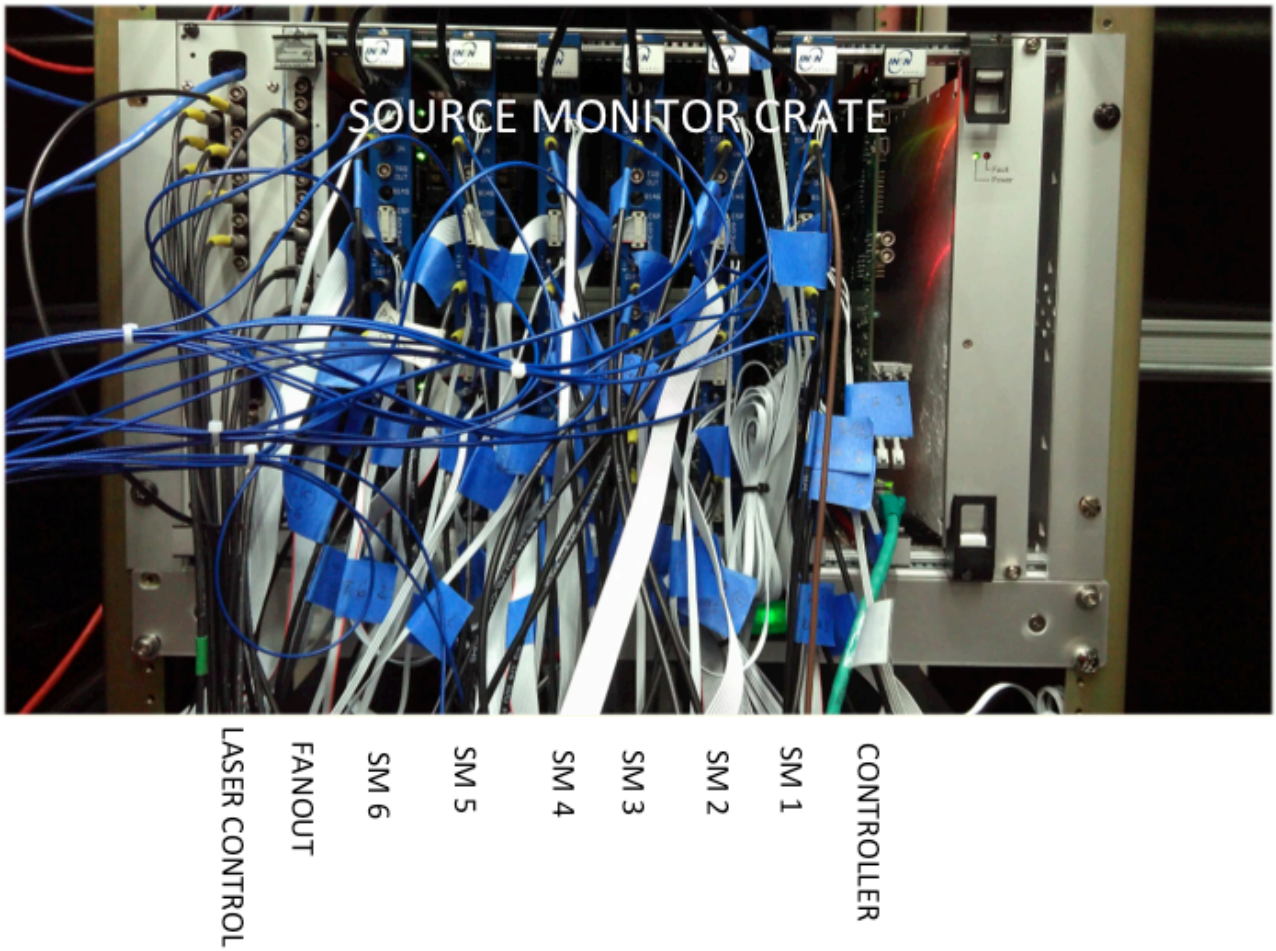

Figure 8: The Source Monitor crate in operation at Fermilab on the Muon g-2 experiment (E989). It contains, from left to right, the Laser Control board, a fast FANOUT unit (100 ps uncertainty) to provide triggers to the 6 lasers, 6 Source Monitor Board and finally the Controller board.

5. Conclusions

A suited Monitoring electronics system has been designed to fulfil the specifications of the high precision Muon g-2 experiment, which started engineering runs last summer. The Laser Control board is in operation, it allows many tests and setup activities of the laser calibration system. The Source Monitor crate is operating and the data acquisition of the laser calibration signals, as well Americium signals, goes on smoothly. The Local Monitor electronics is going to be mounted (1 crate) and the full system will be in operation before summer 2018.

References

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